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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/594,422	09/26/2006	Akira Kitano	160-513	3248

23117 7590 04/05/2010

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EXAMINER	
CARTER, MICHAEL W	

ART UNIT	PAPER NUMBER
2828	

MAIL DATE	DELIVERY MODE
04/05/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/594,422	**Applicant(s)** KITANO ET AL.	
	Examiner MICHAEL CARTER	**Art Unit** 2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,11-17 and 19-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11-17,19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. **Claims 1, 3-4, 6-9, 14-19, and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over US PG Pub 2004/0124500 (Kawagoe) in view of JP Patent 5-190980 (Norihiro) and further in view of US Patent 5,497,391 (Paoli).

3. **For claims 1 and 3**, Kawagoe teaches, a nitride semiconductor laser element comprising: a semiconductor stacked structure including a semiconductor layer of a first conductivity type (figure 1, labels 103-106), an active layer (figure 1, label 107) and a semiconductor layer of a second conductivity type (figure 1, labels 188-111), which are stacked one upon the other and each comprises a nitride (paragraph 28); a striped waveguide region for a laser light provided on the semiconductor layer of the second conductivity type (figure 1, label 111).

4. Kawagoe does not teach an insulative region, formed by implanting ions, for reducing the capacitance of the element, wherein a pn-junction of the semiconductor layer at a peripheral region remote from the waveguide region is broken the insulative region being present remote from at least a portion of an external edge of the semiconductor stacked structure when viewed in plan, said external edge being remote from the striped waveguide region.

5. However, Norihiro teaches an insulative region (figure 1, label 8), formed by implanting ions, for reducing the capacitance of the element, wherein a pn-junction of

the semiconductor layer at a peripheral region remote from the waveguide region is broken (figure 1 and paragraphs 5-6).

6. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the insulating region taught by Norihiro with Kawagoe's laser in order to increase the speed of the laser.

7. The combination does not teach an external edge of the insulative region being remote from an external edge of the active layer when viewed in plan.

8. However, Paoli does teach an external edge of the insulative region (figure 1, label 44) being remote from an external edge of the active layer when viewed in plan (active layer 28 contiues past isolation region 44) in order to form a monolithic array of independently addressable laser (abstract).

9. It would have been obvious to one of ordinary skill in the art at the time the invetnion was made to combine the remote edge of paoli with the previous combination in order to form an array of independently addressable lasers.

10. **For claim 4,** Kawagoe, Norihiro and Paoli are applied as to claims 1 and 3. Further, Kawagoe teaches a substrate (figure 1, label 101), an embedded insulation film covering a side face of the waveguide region and a surface of the semiconductor layer of the second conductivity type (figure 1, label 162), a first electrode in contact with a surface of the waveguide region (figure 1, label 120), a protective insulation film covering at least a part of the embedded insulation film (figure 1, label 164), a second electrode substantially connected to the semiconductor layer of the first conductivity type (figure 1, label 121).

11. **For claim 6,** the combination does not teach the insulative region for reducing the capacitance of the element has a peak of distribution of the impurity concentration in the depth direction in the range from 200 nm to 1 μm from the surface of the semiconductor layer of the second conductivity type.

12. However, it has been held that discovering a workable range involves only routine skill in the art. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to discover the workable range for the depth of implantation in order to form the insulative region as discussed for claim 1.

13. **For claim 7**, the combination teaches the first electrode is formed in contact with the surface of the waveguide region so as to cover a part of the embedded insulation film (figure 1), a pad electrode is formed in contact with the first electrode so as to cover a part of the protective insulation film (figure 1, label 122), and the insulative region for reducing the capacitance of the element includes a region below the embedded insulation film (figure1 of both Kawagoe and Norihiro).

14. **For claim 8,** the combination is applied as to claim 7. Further, the combination teaches the insulation region for reducing the capacitance of the element includes at least the first electrode or a region below the pad electrode (figure1 of both Kawagoe and Norihiro). The combination further teaches the first electrode (Kawagoe, figure 1, label 120 and Norihiro, figure 1, label 9) is formed in contact with the surface of the waveguide region (Kawagoe, figure 1, label 111) so as to cover a part of the embedded insulation pad (Kawagoe, figure 1, label 162) a pad electrode is formed in contact with the first electrode so as to cover a part of the protective insulation film (figure 1, label

122) and the insulative region for reducing the capacitance of the element includes a region below the first electrode or the pad electrode embedded insulation film (figure1 of both Kawagoe and Norihiro).

15. **For claim 9,** Kawagoe teaches the semiconductor laser element is a laser element for emitting bluish-purple light (paragraphs 2 and 5).

16. The combination does not teach the responsiveness of the laser to input of pulse drive current. However, as discussed for claim 1, the combination does teach speeding up a laser. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to set the responsiveness according to the speed required by an application using the laser, and no special significance is given to a response time of 1 ns.

17. **Claim 14** is rejected according to the rejection of claims 1 and 9 above

18. **For claim 15,** the art is applied according to the rejection of claim 8.

19. **For claim 16,** Norihiro further teaches the insulative region for reducing the capacitance of the element is present remote from a resonance surface of the semiconductor laser. Paragraph [0006], 2) states that O+ ions are injected using the SiO_2 stripe as a mask. The mask covers the center portion of the laser and O+ is therefore deposited down the sides of the mask. Portions of the deposition are remote from the resonance surface.

20. **For claim 17, 19 and 21,** the prior art does not explicitly teach the semiconductor stacked structure is rectangular when viewed in plan. However, it is a standard design to form a ridge waveguide laser with a rectangular structure when viewed in plan. It

would have been obvious to one of ordinary skill in the art at the time the invention was made to form a rectangular structure to form an edge emitting device. See for example Nagashima et al. US Patent 6,697,407 (hereinafter referred to as Nagashima) figure 4c. While Nagashima does not show the full structure in plan, it would have been obvious to one of ordinary skill in the art that there is a matching back surface which forms the laser cavity.

21. **Claim 5** remains rejected under 35 U.S.C. 103(a) as being unpatentable over Kawagoe, in view of Norihiro and Paoli, and further in view of US PG Pub 2001/0006529 (Komori).

22. **For claim 5,** Kawagoe, Norihiro and Paoli remain applied as to claim 1.

23. The combination does not teach the insulative region for reducing the capacitance of the element has an impurity peak concentration in the range from $1*10^{18}$ to $5*10^{21}$ atms/cm^3.

24. However, Komori does teach using a concentration $3*10^{18}$ atms/cm^3 in order to create a current blocking layer (paragraph 41).

25. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to determine the workable range, including $3*10^{18}$ atms/cm^3, for impurity concentration in order create a current blocking layer, as discussed for claim 1, since it has been held that discovering a workable range only involves routine skill in the art.

26. **Claims 11-13 and 20** remain rejected under 35 U.S.C. 103(a) as being unpatentable over Kawagoe in view of Paoli and further in view of US Patent 6,697,407

(Nagashima).

27. **For claim 11**, Kawagoe teaches a nitride semiconductor laser element characterized by comprising: a semiconductor layer of a first conductivity type (figure 1, labels 103-106), an active layer (figure 1, label 107) and a semiconductor layer of a second conductivity type being different from the first conductivity type (figure 1, labels 188-111), which are stacked on a main surface of a substrate and each comprises a nitride (paragraph 28); and a striped waveguide region for a laser light provided on the semiconductor layer of the second conductivity type (figure 1, label 111).

28. Kawagoe does not teach wherein at least a part of the semiconductor layer of the second conductivity type serves as a region for reducing the capacitance of the element by being converted into the first conductivity type in a direction of thickness at a peripheral region remote from at least a portion of an external edge remote from the waveguide region.

29. However, Nagashima does teach at least a part of the semiconductor layer of the second conductivity type serves as a region for reducing the capacitance of the element by being converted into the first conductivity type in a direction of thickness at a peripheral region remote from the waveguide region (figure 1, label 30) in order to form a current blocking layer (column 10, lines 33-38). Nagashima further teaches the region of the second conductivity type (figure 1, label 26) between the regions of the first conductivity type (figure 1, labels 30) shows the region for reducing capacitance is remote from at least a portion of an external edge remote from the waveguide region.

30. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to convert part of the second type layer in Kawagoe into a first type layer according to Nagashima in order to form a current blocking layer.

31. The combination does not teach an external edge of the insulative region being remote from an external edge of the active layer when viewed in plan.

32. However, Paoli does teach an external edge of the insulative region (figure 1, label 44) being remote from an external edge of the active layer when viewed in plan (active layer 28 contiues past isolation region 44) in order to form a monolithic array of independently addressable laser (abstract).

33. It would have been obvious to one of ordinary skill in the art at the time the invetnion was made to combine the remote edge of paoli with the previous combination in order to form an array of independently addressable lasers.

34. **For claim 12**, Nagashima further teaches an npn structure (figure 1, labels 21, 29, and 30) in the peripheral region remote from the waveguide region, wherein the semiconductor layer of the first conductivity type is an n-type semiconductor layer, and the semiconductor layer of the second conductivity type is a p-type semiconductor layer.

35. **For claim 13**, Nagashima further teaches a pnpn structure (figure 1, labels 21, 29, 30, and 31) in the peripheral region remote from the waveguide region, wherein the semiconductor layer of the first conductivity type is an n-type semiconductor layer, and the semiconductor layer of the second conductivity type is a p-type semiconductor layer.

36. **For claim 20**, the prior art does not explicitly teach the semiconductor stacked structure is rectangular when viewed in plan. However, it is a standard design to form a

ridge waveguide laser with a rectangular structure when viewed in plan. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a rectangular structure to form an edge emitting device. See for example Nagashima et al. US Patent 6,697,407 (hereinafter referred to as Nagashima) figure 4c. While Nagashima does not show the full structure in plan, it would have been obvious to one of ordinary skill in the art that there is a matching back.

37. **Claims 22-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawagoe, Norihiro and Paoli and further in view of US 6,291,256 (Chen) in view of US 6,881,324 (Morse).

38. **For claim 22 and 23**, the previous combination does not teach a plurality of the insulative region are provided along the striped waveguide region, spaced from each other and wherein the insulative region is provided so that portion thereof facing the waveguide region is rugged.

39. However, Chen does teach forming a grating with a plurality of regions provided along the striped waveguide region, spaced from each other (figure 7, label 20) in order to from a DFB laser grating (abstract). Chen does not teach the regions are insulative regions. However, Morse does teach a grating may be formed by implanting ions (column 1, lines 57-61 and figure 5c) as an alternative to etching.

40. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine regions provided along the striped waveguide region, spaced from each other as taught by Chen and Morse with the previous combination in order to form a DFB grating. Further, it would have been obvious to use the ions

already present in Kawagoe, rather than adding additional implant steps, which make the regions insulative.

41. Providing the grating as discussed above forms the insulative region so that portion thereof facing the waveguide region is rugged.

Response to Arguments

42. Applicant's arguments with respect to claim 1, 4, 11 and 14 have been considered but are moot in view of the new grounds of rejection necessitated by amendment.

Conclusion

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL CARTER whose telephone number is (571)270-1872. The examiner can normally be reached on Monday-Friday, 7:00 a.m.-4:30 p.m., EST.

44. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571) 272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

45. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MC/

/Minsun Harvey/
Supervisory Patent Examiner, Art Unit 2828